REMARKS

The application has been reviewed in light of the Office Action dated October 15, 2008. Claims 19, 20 and 22-40 were pending, with claims 1-18 and 21 having previously been canceled, without prejudice or disclaimer. By this Amendment, claims 19 and 20 have been canceled, without prejudice or disclaimer, claims 22 and 31 have been amended to clarify the claimed subject matter, and new claim 41 has been added. Claims 22-41 would be pending upon entry of this amendment, with claims 22 and 31 being in independent form.

Claims 22-24 and 30-33 were rejected under 35 U.S.C. §102(e) as purportedly anticipated by Chu et al (US 2004/0015731 A1). Claims 25, 26, 29 and 34-36 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Chu in view of U.S. Patent No. 6,470,439 to Yamada. Claims 27, 28, 37 and 38 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Chu in view of Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang. Claims 19, 20, 39 and 40 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Chu in view of U.S. Patent No. 6,528,974 to Mirov.

Applicant respectfully submits that the present application is allowable over the cited art, for at least the reason that the cited art does not disclose or suggest the aspects of the present application that the first memory stores ***first information indicating specific addresses of corresponding specified registers in the register circuit***, and the second memory stores ***second information corresponding to said data*** read by said optical disk drive mechanism from said optical disk medium, ***to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory***.

Chu, as understood by Applicant, proposes a method and system for reducing power consumption in a hard disk drive (HDD), such as shown in Fig. 3 (reproduced below) of Chu, in

situations where a host device writes data to or reads data from the drive.

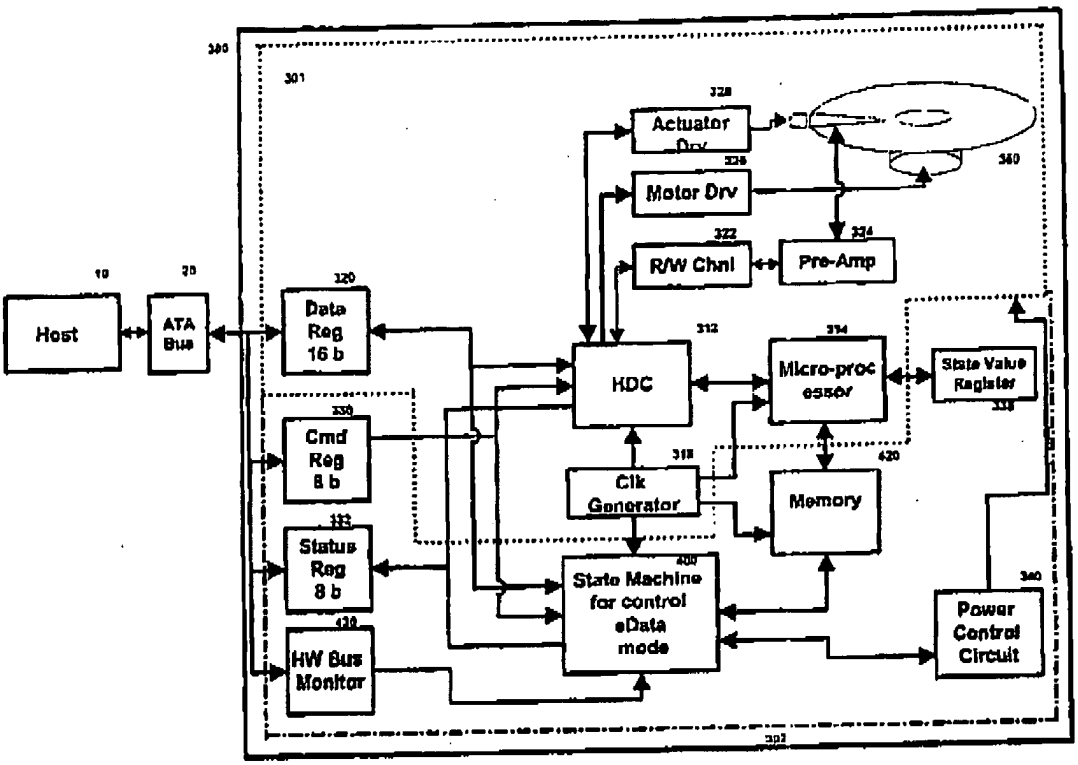

Figure 3

The 16-bit data register 320 of Chu is equated in the Office Action with the register circuit of the present application, the memory 420 of Chu is equated in the Office Action with both the first memory and second memory of the present application, and state machine 400 is equated in the Office Action with the control circuit of the present application.

However, Chu does not disclose or suggest a first memory configured to store first information indicating specific addresses ***of corresponding specified registers in the register circuit***.

As previously discussed in the record, while the memory 420 of Chu can be configured to include a Logical Block Address (LBA) counter, such LBA counter has nothing to do with

specific addresses of the 16-bit data register 320 of Chu (which is equated in the Office Action to the register circuit of the present application).

Chu, [0038] (reproduced below) is cited in the Office Action in connection with the contention that the LBA counter is "used to store the starting address of the data" and stores the addresses of the corresponding registers in the register circuit (i.e. the addresses in which the read data will be stored after it is buffered).

> [0038] Flow continues to step 506 where it is determined whether the received command is for a write operation or for a read operation. ***If the command is a write operation, flow continues to step 507 where a write cache and various counters are configured and enabled within Memory 420, i.e., the LBA counter, the data size counter***, the cache buffer available size counter, and the host data access frequency counter. ***The LBA counter is used to store the starting address of the data. The data size counter is used to store the number of LBAs.*** The Cache buffer available size counter holds available capacity of the cache buffer after each cache write operation. The Host data access frequency counter is used to determine how often is host performs write operation.

However, as clearly evident from Chu, [0038], the LBAs in Chu refer to the starting address of the data in the in the hard disk itself, NOT the starting address of the data in the register circuit. Indeed, it is well known in the art, especially with respect to ATA/ATAPI interface standards for connection of storage devices in computers, that LBA (Logical Block Addressing) is the scheme used to specify the location of blocks of data in the storage devices themselves i.e. in the hard disk. Since Chu provides for a read cache to reproduce data corresponding to the data in the HDD, the skilled artisan would understand that the read cache employs Logical Block Addressing so that this reproduced data can be identified. For example, if the Host computer is looking for data stored in the hard disk starting at Logical Block Address = 7, then any cache entry of this data must also provide the same tag i.e. Logical Block Address = 7, so that this data can be correctly identified, accessed and retrieved.

Moreover, the write cache in Chu (which stores data coming *from* the host computer and to be written/sent *to* the hard disk drive) also uses the LBAs, in order to specify the corresponding location in the hard disk where such data needs to be written to. Indeed, Chu, [0038], in fact refers to the write procedure of the write cache (i.e. steps 507-510 in Figure 5), not the read procedure of the read cache. Clearly, the write cache of Chu is not storing the starting address of the data in the register circuit. Rather, the write cache of Chu is using the LBA scheme to store "the starting address of the data" in the hard disk, so that the data in the write cache can be written *to* the hard disk at the appropriate destination represented by the corresponding LBA tag.

It is clear that the read cache in Chu is utilizing the same LBA scheme as the write cache in Chu. Chu, [0028], is reproduced below:

> [0028] When Host 1 issues a data read command, **and all of the requested data is stored in Read Cache 140 or Write Cache 130**, then the State Machine 120 returns the requested data to Host 1 without affecting the power state of Device 2. **If any of the requested data is not stored in Read Cache 140 or Write Cache 130**, then eData State Machine 120 will issue the necessary read commands over Device Interface 150 to read the appropriate data from Device 2 and send it to Host 1. Once Device 2 has satisfied the read requests, eData State Machine 120 is able to perform additional read operations to fill up Read Cache 140, or to flush Write Cache 130. One of the most common techniques is the read ahead operation, in which more data is read from Device 2 following the last data request by Host 1.

For example, if the write cache is already storing data to be written in the hard disk starting at Logical Block Address = 7, and the Host computer is looking for data stored in the hard disk starting at Logical Block Address = 7, the read cache must be accessed in order to determine if such data is already stored there, **and** the write cache must be accessed in order to determine if the specified data is stored there. Hence, the write and read cache (as well as the hard disk) of Chu, must use the same LBA scheme, in order to correctly identify and handle

information.

Thus, the LBAs in Chu refer to the starting address of data in the HDD, not to the starting address of data in the 16-bit data register 320, as contended in the Office Action. Accordingly, the memory 420 of Chu does NOT store first information indicating specific addresses ***of corresponding specified registers in the register circuit***, or second information ***to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory***.

Applicant submits that the cited art, even when considered along with common sense and common knowledge to one skilled in the art, simply does ***NOT*** render unpatentable the aspects of the present application that the first memory stores ***first information indicating specific addresses of corresponding specified registers in the register circuit***, and the second memory stores ***second information corresponding to said data*** read by said optical disk drive mechanism from said optical disk medium, ***to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory***.

Accordingly, applicant submits that independent claims 22 and 31, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any required fees, and credit any overpayment, to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400